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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/014,584	12/14/2001	Tomoyuki Furuhata	15.57/6348	2011

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KONRAD RAYNES VICTOR & MANN, LLP
Suite 210
315 South Beverly Drive
Beverly Hills, CA 90212

EXAMINER	
MANDALA, VICTOR A	
ART UNIT	PAPER NUMBER
2826	8

DATE MAILED: 02/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/014,584	FURUHATA, TOMOYUKI	
	Examiner	Art Unit	
	Victor A Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *4, 6-9, 12-17, 21-22, & 27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 5, 10-11, 18-20, 23-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restriction

1. Examiner has noted that the applicant has responded to the election restriction from the last communication response, Paper No. 7, filed 1-16-03. The applicant has elected Species I, of Figures 1-3, 6-11, 14, and 16 claims 1-3, 5, 10-11, 18-20, and 23-26 for further examination without traverse. The restriction is made final. Examiner disagrees with the applicants that there are no generic claims and applicant has not supported their arguments on which claim is believed to be generic.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

2. Claims 18 & 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The examiner is unable to understand the Applicant's invention where in claim 18 a second circuit region **mix-mounted** therein.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 11, 18, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,274,907 Nakagawa.

3. Referring to claim 1, a semiconductor device having a non-volatile memory transistor, comprising: a semiconductor layer, (Figure 24a #5); a floating gate, (Figure 24a #31), disposed over the semiconductor layer, (Figure 24a #5), through a first dielectric layer as a gate dielectric layer, (Figure 24a #25); a second dielectric layer, (Figure 24a #35), that contacts at least a part of the floating gate, (Figure 24a #31), and is capable of functioning as a tunneling dielectric layer; a control gate, (Figure 24a #41), formed over the second dielectric layer, (Figure 24a #35); and an impurity diffusion layer that forms a source region, (Figure 24a #51), or a drain region, (Figure 24a #55), formed in the semiconductor layer, (Figure 24a #5), wherein a conduction layer, (Figure 21a #76a), is provided above the floating gate, (Figure 24a #31), and the conduction layer, (Figure 21a ~~#76a),~~ 81 entirely overlaps the floating gate, (Figure 24a #31).

4. Referring to claim 3, a semiconductor device having a non-volatile memory transistor, wherein a side end of the conduction layer, (Figure 21a #76a), formed above the floating gate, (Figure 24a #31), and an end of the floating gate, (Figure 24a #31), are aligned with each other.

5. Referring to claim 11, a semiconductor device having a non-volatile memory transistor, comprising a non-volatile memory transistor including a semiconductor layer, (Figure 24a #5), a floating gate, (Figure 24a #31), disposed above the semiconductor layer, (Figure 24a #5), and a control gate, (Figure 24a #41), formed above the floating gate, (Figure 24a #31), wherein a conduction layer, (Figure 21a #81), is provided above the non-volatile memory transistor and a portion of the conduction layer, (Figure 21a #81), is located vertically above the floating gate, (Figure 24a #31), and a width of the conduction layer, (Figure 21a #81), located vertically above the floating gate, (Figure 24a #31), is formed to be greater than a width of the floating gate, (Figure 24a #31).

6. Referring to claim 18, a semiconductor device having a non-volatile memory transistor, wherein the non-volatile memory transistor comprises a first circuit region, (Figure 24a Examiner's label #254), and wherein the semiconductor device further comprises a second circuit region, (Figure 24a #255), mix-mounted therein.

7. Referring to claim 20, a semiconductor device having a non-volatile memory transistor, further comprising: a first dielectric layer, (Figure 24a #25), that defines a gate dielectric layer disposed between the semiconductor layer, (Figure 24a #5), and the floating gate, (Figure 24a #31); a second dielectric layer, (Figure 24a #35), that contacts at least a part of the floating gate, (Figure 24a #31), and is capable of functioning as a tunneling dielectric layer; and an impurity diffusion layer that forms a source region, (Figure 24a #51), or a drain region, (Figure 24a #55), formed in the semiconductor layer, (Figure 24a #5).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 & 5 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,100,579 Sonoda et al.

8. Referring to claim 1, a semiconductor device having a non-volatile memory transistor, comprising: a semiconductor layer, (Figure 13 #50); a floating gate, (Figure 13 #52), disposed over the semiconductor layer, (Figure 13 #50), through a first dielectric layer as a gate dielectric layer, (Figure 13 #54); a second dielectric layer, (Figure 13 #60), that contacts at least a part of the floating gate, (Figure 13 #52), and is capable of functioning as a tunneling dielectric layer; a control gate, (Figure 13 #53), formed over the second dielectric layer, (Figure 13 #60); and an impurity diffusion layer that forms a source region, (Figure 13 #55), or a drain region, (Figure 13 #56), formed in the semiconductor layer, (Figure 13 #50), wherein a conduction layer, (Figure 13 #58), is provided above the floating gate, (Figure 13 #52), and the conduction layer, (Figure 13 #58), entirely overlaps the floating gate, (Figure 13 #52).

9. Referring to claim 5, a semiconductor device having a non-volatile memory transistor, wherein the conduction layer, (Figure 13 #58), is electrically connected to the semiconductor layer, (Figure 13 #50 via #55).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 23 & 24 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,959,879 Koo.

10. Referring to claim 1, a semiconductor device having a non-volatile memory transistor, comprising: a semiconductor layer, (Figure 2 #100); a floating gate, (Figure 2 #112), disposed over the semiconductor layer, (Figure 2 #100), through a first dielectric layer as a gate dielectric layer, (Figure 2 #110); a second dielectric layer, (Figure 2 #114), that contacts at least a part of the floating gate, (Figure 2 #112), and is capable of functioning as a tunneling dielectric layer; a control gate, (Figure 2 #116), formed over the second dielectric layer, (Figure 2 #114); and an impurity diffusion layer that forms a source region, (Figure 2 #106), or a drain region, (Figure 2 #108), formed in the semiconductor layer, (Figure 2 #100), wherein a conduction layer, (Figure 2 & 4 #118), is provided above the floating gate, (Figure 2 & 4 #112), and the conduction layer, (Figure 2 & 4 #118), entirely overlaps the floating gate, (Figure 2 & 4 #112).

11. Referring to claim 10, a semiconductor device having a non-volatile memory transistor, comprising: a non-volatile memory transistor including a semiconductor layer, (Figure 2 #100), a floating gate, (Figure 2 #112), disposed above the semiconductor layer, (Figure 2 #100), and a control gate, (Figure 2 #116), formed to extend above a portion of the floating gate, (Figure 2

#112), wherein a conduction layer, (Figure 2 #118), is provided vertically above the floating gate, (Figure 2 #112), at least in a region where the control gate, (Figure 2 #116), is not disposed vertically above the floating gate, (Figure 2 #112).

12. Referring to claim 23, a semiconductor device having a non-volatile memory transistor, comprising a semiconductor layer, (Figure 2 #100); a floating gate, (Figure 2 #112), disposed over the semiconductor layer, (Figure 2 #100), through a first dielectric layer comprising a gate dielectric layer, (Figure 2 #110); a second dielectric layer, (Figure 2 #114), that contacts at least a part of the floating gate, (Figure 2 #112), and is capable of functioning as a tunneling dielectric layer; a control gate, (Figure 2 #116), formed over the second dielectric layer, (Figure 2 #114); and one or more conduction layers, (Figure 2 #118), formed over the floating gate, (Figure 2 #112), the floating gate, (Figure 2 #112), including an upper surface, wherein a line normal to any portion of the upper surface will contact at least one of the one or more conduction layers, (Figure 2 & 4 #118), over the floating gate, (Figure 2 & 4 #112).

13. Referring to claim 24, a method for manufacturing a semiconductor device having a non-volatile memory transistor, comprising: forming a first dielectric layer, (Figure 2 #110), comprising a gate dielectric layer, (Figure 2 #110), on a substrate, (Figure 2 #100); forming a floating gate, (Figure 2 #112), over the gate dielectric layer, (Figure 2 #110); forming a second dielectric layer, (Figure 2 #114), that contacts at least a part of the floating gate, (Figure 2 #112), and is capable of functioning as a tunneling dielectric layer; forming a control gate, (Figure 2 #116), over the second dielectric layer, (Figure 2 #114); forming an impurity diffusion layer that forms a source region, (Figure 2 #106), or a drain region, (Figure 2 #108), in the semiconductor layer; and forming a conduction layer, (Figure 2 #118), above the floating gate, (Figure 2 #112),

so that a portion of the conduction layer, (Figure 2 & 4 #118), is positioned vertically above the floating gate, (Figure 2 & 4 #112), where the portion of the conduction layer, (Figure 2 & 4 #118), overlaps the entire floating gate, (Figure 2 & 4 #112).

14. Referring to claim 25, a method for manufacturing a semiconductor device having a non-volatile memory transistor, comprising: forming a floating gate, (Figure 2 #112), above a semiconductor layer, (Figure 2 #100); forming a control gate, (Figure 2 #116), that extends above a portion of the floating gate, (Figure 2 #112); and forming a conduction layer, (Figure 2 #118), vertically above the floating gate, (Figure 2 #112), at least in a region where the control gate, (Figure 2 #116), is not disposed vertically above the floating gate, (Figure 2 #112).

15. Referring to claim 26, a method for manufacturing a semiconductor device having a non-volatile memory transistor, comprising: forming the conduction layer, (Figure 2 #118), to have a width greater than that of the floating gate, (Figure 2 #112), in a region where the conduction layer, (Figure 2 #118), is disposed vertically above the floating gate, (Figure 2 #112).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,959,879 Koo.

16. Referring to claim 2, a semiconductor device having a non-volatile memory transistor, wherein the conduction layer, (Figure 2 & 4 #118), outwardly protrudes from an end of the floating gate, (Figure 2 #112), as viewed in a plan view, and a width of a portion of the conduction layer, (Figure 2 & 4 #118), that outwardly protrudes from the end of the floating gate, (Figure 2 & 4 #112), as viewed in a plan view is 0.5 μm or smaller.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (703) 308-6560. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

VAMJ
January 28, 2003